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A SINGLE-BIT DIGITAL NON-COHERENT BASEBAND BFSK DEMODULATOR

Adam Charles Thompson[†], Zahir M. Hussain[†], and Peter O'Shea[‡]

[†]School of Electrical and Computer Engineering,
RMIT University, Melbourne, Victoria, Australia

Emails: s2114313@student.rmit.edu.au and zmhussain@ieee.org

[‡]School of Electrical and Electronic Systems Engineering,
Queensland University of Technology, Brisbane, Australia

Email: pj.oshea@qut.edu.au

ABSTRACT

Recently we have presented efficient structures for filters that produce an output with a single-bit resolution. As an application and extension of these works a baseband digital single-bit non-coherent Binary Frequency Shift Keying (BFSK) demodulator is proposed. This new structure contains no multi-bit multiplications unlike traditional methods of digital BFSK demodulation. The single-bit BFSK demodulator is then simulated using an additive white gaussian noise channel. As a benchmark the single-bit BFSK demodulator and the theoretical non-coherent BFSK demodulator bit errors are calculated and compared.

1. INTRODUCTION

The proliferation of Sigma-Delta data converters currently available on the market suggests that it is a popular choice of conversion element. The oversampled single-bit format produced by sigma-delta analog-to-digital conversion is generally resampled to the Nyquist rate then filtered to produce the traditional multi-bit output [1]. This filtering removes the quantization noise introduced by the coarse, often single-bit, quantization. Once filtered, traditional digital-signal-processing operations are used to manipulate the signal.

However, the advantages of keeping a data converters output in the single-bit format are only recently being explored [2][3][4][5]. As the single-bit format alphabet is composed of only two symbols $\{-1,1\}$, the multiplication operation becomes trivial; implementation can be realized with either a multiplexor or a couple of logic gates [6]. This is the converse of the multi-bit multiplication that requires complex logic. The single-bit format requires much less internal signal-routing within field programmable gate arrays (FPGA) or integrated circuits as compared to the multi-bit alternative. Finally, sigma-delta analog-to-digital converters can be made simpler as the decimation and filtering stages are no longer required. This decrease in com-

plexity implies reduced silicon space requirements in implementation of single-bit systems.

In this paper we propose the use of single-bit techniques to demodulate a baseband Binary Frequency Shift Keying (BFSK) signal. We assume that the signals at the input to such a demodulator are at baseband frequencies; or equivalently may have been transmitted in this form within a digital system.

Matched filters and coherent detection systems in BFSK will provide greater signal to noise ratios and hence, lower probabilities of error at the receiver. However, coherent detection normally requires phase synchronization between the carrier signal and the local oscillators at the receiver. Typically, phase synchronization circuits are required; such synchronization circuits are complex. Hence, many BFSK receivers employ a non-coherent demodulator. The proposed demodulator will be of the non-coherent type. A block diagram of a non-coherent BFSK demodulator is shown in Figure 1.

Fig. 1. Block diagram of a non-coherent BFSK demodulator.

This BFSK demodulator employs two narrowband finite impulse response (FIR) filters. The center frequencies of the filters are set to ω_1 and ω_2 where the basis functions generated at the transmitter are $\cos(\omega_1 t)$ and $\cos(\omega_2 t)$ and t represents time and ω radian frequency. An envelope detector is used to generate a DC level from each narrowband filter. The resultant DC levels are then added and passed to a threshold detector that determines which level, and hence which frequency, was received.

This structure can be made more efficient through the use of single-bit filtering [2] [7] and through the

provision of a single-bit output [3]. We propose a BFSK demodulator that can use either a single- or multi-bit word input that efficiently produces a single-bit demodulated output.

2. THE SINGLE-BIT BFSK DEMODULATOR

The structure of the proposed single-bit BFSK demodulator is shown in Figure 2. The structure is similar to the traditional non-coherent demodulator shown in Figure 1.

Fig. 2. Block diagram of the efficient non-coherent BFSK demodulator.

The bandpass ternary FIR filters are efficient filters that have coarsely quantized filter coefficients. The filtered signals from each frequency branch are rectified (any sample less than zero is set to zero) whilst they are in the multi-bit format produced by the ternary filter. Remodulation then puts the rectified signals into the single-bit format. This reduces the complexity of the subtraction of the two frequency branches. The subtractor output is then multiplied by a gain and remodulated to the single-bit format. The multiplication and subtraction operation can be implemented with a small lookup table to keep the system efficient.

3. THE TERNARY FIR FILTER

The ternary filter is an FIR filter with a reduced coefficient alphabet. The ternary filter coefficients, or taps, are restricted to the set $\{-1, 0, 1\}$. Mathematically, the FIR filter output $y(k)$ can be described by the convolution of the ternary taps h_i and the input signal $x(k)$. Given M as the order of the FIR filter, the output of the ternary filter would be

$$y(k) = \sum_{i=0}^M h_i x_{k-i}, \quad h_i \in \{1, 0, -1\}. \quad (1)$$

The structure of the ternary FIR filter is shown in Figure 3. The limited tap values allow for a simple hardware implementation. Multiplication in the single-bit domain can be achieved with a couple of logic gates or a simple lookup table [6]. As for the zero in the ternary alphabet, it is simply implemented with a delay and no input to the final summer within the ternary filter is required. After many simulation studies the authors found that up to half of the tap values for simple lowpass filters could be zero. This significantly reduces the number of bits required at the output of the

summer and makes ternary filters simple and efficient in hardware implementation.

The authors use Sigma-Delta modulation of a target impulse response to generate the ternary taps [2][8][9]. The double loop $\Sigma\Delta m$ shown in Figure 4 was used due to its implementation simplicity. Higher order modulators will produce filters with higher stopband attenuations however, such high stopband attenuation is not needed in this application. The z -domain transfer function of the double loop $\Sigma\Delta m$ is given by [1]:

$$H(z) = G(z)z^{-1} + E(z)(1 - 2z^{-1} + z^{-2}) \quad (2)$$

where $G(z)$ represents the target impulse response and $E(z)$ represents the quantization noise transfer functions. The noise shaping effect of the $\Sigma\Delta m$ is evident from the presence of the filtering term, $(1 - 2z^{-1} + z^{-2})$, acting on the noise term, $E(z)$. The frequency response of the above $\Sigma\Delta m$ is given by:

$$H_{\Sigma\Delta T}(e^{j\Omega}) = G(e^{j\Omega})e^{-j\Omega} + E(e^{j\Omega})(1 - 2e^{-j\Omega} + e^{-2j\Omega}) \quad (3)$$

where Ω is the normalized radian frequency.

Fig. 3. Block diagram of ternary FIR filter.

4. RECTIFICATION AND REMODULATION

Rectification is preformed at the output of the ternary FIR filter. This rectification can be implemented with a multiplexor. The multiplexor outputs either the input signal or sets the output to zero depending on the state of the sign-bit. If the sign-bit is positive or zero it outputs the signal at the input else if the input has a negative sign-bit the multiplexor outputs zero. Hence, the rectification operation is achieved efficiently.

The multi-bit output from the rectifier is then remodulated back to single-bit. This remodulation takes place to simplify the subtraction and following multiplication as shown in Figure 2. The double loop $\Sigma\Delta m$ is used to remodulate the signal because it performs well and has a simple implementation that contains only summers, delays and a quantizer. The structure of the double loop $\Sigma\Delta m$ used in the BFSK demodulator is shown in figure 4. The system transfer function is given in equation 2.

A.G. **1 1 0 0 0 0 0 0 0 0 1 1 0 0 1**

5. RESULTS AND DISCUSSION

Before simulations can begin the bandpass ternary filters taps are required. The method in [2] was used to generate the taps. Firstly the passband response $P(f)$ is

The simulation was performed at an oversampling ratio of 128 and the symbol rate was set as 1000 sam-

sary to place the demodulator output in the baseband

Input Binary Data

The graph of the the total demodulator errors and

Fig. 7. Bit error rate Vs symbol to noise powers ratio.

total number of sample ratio versus symbol energy to noise power ratio is shown in Figure 7. As a comparison, the theoretical probability of error (P_e) for a non-coherent BFSK demodulator is also plotted [10]. The equation of the P_e theoretical line is:

$$P_e = \frac{1}{2} \exp \left(-\frac{A^2}{4N_o W_f} \right) \quad (4)$$

where A is the input sinusoid amplitude, N_o is the power spectral density of the input noise and W_f is the bandwidth of the bandpass filters.

The simulated and theoretical graphs in Figure 7 show good correlation, particularly at the lower E_s/N_o . The theoretical graph shows the probability of error being lower at $E_s/N_o=15$ dB. The cause of this deviation may be due to in-band noise created from the remodulation operations within the single-bit demodulator. This effect may be reduced if the system sampling frequency is increased. Alternatively a $\Sigma\Delta m$ with better noise shaping ability may also improve the bit error rate at higher E_s/N_o ratios. These options requires further investigation. The authors also found that increasing the symbol sample rate above 1000 samples/sec caused an increase in the bit error rate at the demodulator output.

6. CONCLUSIONS

A non-coherent digital single-bit binary frequency shift keying demodulator was presented. Through the use of single-bit processing techniques this new structure was able to successfully demodulate BFSK signals with a single-bit output. The structure, although similar to the traditional non-coherent BFSK demodulator, contains no multi-bit multiplications. This greatly reduces the implementation complexity of the single-bit system.

The demodulator performance was briefly investigated through the use of an AWGN channel and determination of errors at the demodulators output. The

signal energy to noise power ratio was varied from 15 to -10 dB to describe the error performance with an increasingly noise degraded signal. The simulated and theoretical graphs show good correlation at lower E_s/N_o . Further investigation is required to determine the bit error rates at different symbol rates and with different oversampling ratios.

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