A single-bit digital DC-blocker using ternary filtering

Sadik, Amin; Hussain, Zahir; O'Shea, Peter

https://researchrepository.rmit.edu.au/esploro/outputs/9921859301701341/filesAndLinks?institution=61RMIT_INST&index=null

Sadik, A., Hussain, Z., & O'Shea, P. (2005). A single-bit digital DC-blocker using ternary filtering. Proceedings of the TENCON 2005 IEEE Region 10 Conference, 1–6.
<https://doi.org/10.1109/TENCON.2005.301222>

Published Version: <https://doi.org/10.1109/TENCON.2005.301222>

Repository homepage: <https://researchrepository.rmit.edu.au>

© 2005 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

Downloaded On 2023/04/26 20:28:40 +1000

A Single-Bit Digital DC-Blocker Using Ternary Filtering

Amin Z. Sadik

School of Engineering Systems
Queensland University of Technology
Currently a Visiting Researcher at SECE
RMIT, Melbourne, Australia
E-mail: amin.sadik@rmit.edu.au

Zahir M. Hussain, SMIEEE

School of Electrical & Computer Engineering
RMIT, Melbourne, Australia
Email: zmhussain@ieee.org

Peter O'Shea

School of Engineering Systems
Queensland University of Technology
Brisbane, Australia
pj.oshea@qut.edu.au

Abstract—In this paper, a single-bit dc-blocker is presented. It is comprised of a ternary filtering stage preceded by a sigma-delta modulator. Different techniques are used to generate the ternary taps for hardware and performance optimization. Both the input and the output of this dc-blocker are assumed in single-bit format. The proposed dc-blocker can easily be implemented with FPGA.

I. INTRODUCTION

Single-bit $\Sigma\Delta$ modulators have found an increasing number of applications in audio and other digital signal processing (DSP) systems due to their efficient hardware implementation. However, the design of single-bit systems is a non-trivial task, which is prone to many unresolved issues. One of these problems is the undesired DC components that can be introduced into the bitstream at various stages.

$\Sigma\Delta$ modulators ($\Sigma\Delta$ M's) are the core elements in single-bit digital systems. The performance of a $\Sigma\Delta$ M deteriorates when it is driven by DC-biased signals, as this will affect its dynamic range and enhance unwanted limit cycles, therefore, affect the overall system stability. However, in practice, some of these limit cycles are necessary for the correct operation of $\Sigma\Delta$ modulator. These are known as idle patterns, which usually have frequencies located faraway from the baseband, and therefore, can easily be disturbed by applying an input to the system [1]. On the other hand, large signal limit cycles have stable or diverging amplitudes with frequencies often located near the baseband. Therefore, it is very difficult, if not impossible, to disturb these cycles, which are audible in audio applications [2].

Of course, the DC content can easily be removed from multi-bit signals by using traditional DC cancellers [3], i.e., before encoding to single-bit format. The problem, however, arises when a DC component appears in the single-bit encoded signal. In this case, removing this DC component is a vital design task.

In this paper, a single-bit digital DC-blocker is designed, simulated and assessed in terms of the extent of DC elimination and signal-to-noise-ratio. The proposed DC-blocker is efficient in hardware implementation.

II. THEORY AND DESIGN

A. The Ternary Filtering Stage

In fact, the key issue here is the design of the ternary filter. The ternary filter is a FIR filter with coefficients confined to the ternary set: $\{-1, 0, +1\}$. As the input to the ternary filter

Fig. 1. Structure of the ternary filter.

is in single-bit format, hardware implementation will be significantly efficient in the sense that each multiplication operation can be implemented with either a couple of logic gates or a simple look-up table [4]. The structure of the ternary filter is shown in Fig.(1). There are several algorithms to generate the ternary tap coefficients from a specific target impulse response, such as dynamic programming and mini-max techniques [5],[6]. However, in this work, the tap values are encoded using $\Sigma\Delta$ modulation of a target impulse response. The digital $\Sigma\Delta$ used for this purpose must satisfy two conditions. Firstly, it must have a tri-level output $\{-1, 0, +1\}$. Second, the $\Sigma\Delta$ modulator must have a flat signal frequency response over the bandwidth of interest [7]. This implies that the $\Sigma\Delta$ modulator should not modify the specifications of the target impulse response. The ternary filter requires operation at an oversampled rate (OSR). This requirement will be satisfied as the input signal is assumed here to be a $\Sigma\Delta$ modulated bit-stream.

The ternary filter, however, has two pitfalls. First, it provides a multi-bit output, hence, re-modulating is necessary. Second, it suffers from high-frequency noise because of the harsh quantization of both the input signal and the target impulse response. To resolve the first problem and alleviate the second one, a second-order $\Sigma\Delta$ modulator is presented. Moreover, this modulator stage should provide good noise-shaping at low OSR's to reduce the number of the ternary filter taps, and consequently, lower the filter order needed to maintain the target response. However, despite the attempts that has been made to derive a relationship which can predict the performance of ternary filtering during the design stage, no one of these attempts were particularly successful.

However, before completing the ternary filter design, it is only possible to anticipate its performance in terms of average and worst case stop-band attenuation. Back again to the design of

Fig. 2. Frequency response of ideal multi-bit dc blocker for different values of the gain parameter $\alpha=0.5, 0.9$, and 0.995 .

the ternary filter. We start with the transfer function of an ideal multi-bit dc-blocker which can be given as follows [8]:

$$H(z) = \frac{1 - z^{-1}}{1 - \alpha z^{-1}} \quad (1)$$

DC blocking is due to the zero of the above transfer function at $z = 1$ (0 Hz). The pole at $z = \alpha$ controls the system bandwidth, and therefore, the system transit response. Fig.(2) depicts the frequency response based on eq.1 for various values of the gain parameter α . As $\alpha \rightarrow 1$, the notch at dc gets narrower. This may seem ideal, however, there is a drawback. When $\alpha \rightarrow 1$, the impulse response duration will increase. Fortunately, as the end of the impulse response gets longer, its initial amplitude decreases. When $\alpha = 1$, the pole and zero cancel each other at all frequencies, and hence, the impulse response shrinks to an impulse and the notch disappears.

A suitable target response can be designed such that it presents dominant zeros on the 0 Hz axis in the z-plane. Different FIR design techniques can be employed to generate its full-precision coefficients as will be seen later. These target filter coefficients are then interpolated by a factor of OSR using the FFT technique. The ternary filter output $u(k)$ is given by the convolution of ternary taps $h(i)$ (or simply h_i) and the input signal $x(k)$ as follows:

$$u(k) = \sum_{i=0}^M h_i x_{k-i} \quad (2)$$

where $M + 1$ is the order of the filter.

It is vital here to realize that the design in single-bit oversampling domain is not straightforward as is the case in multi-bit domain. For instance, in our case where a dc blocker is intended to be designed, the problem of accurate discrimination between the dc content and the time-varying signal component will arise. This is due to the large oversampling ratio (32 or more) that practically pushes the time-varying signal spectrum to the vicinity of 0 Hz in the normalized frequency domain. As such an ultimate care should be given to alleviate strong attenuation and avoid the possible differentiation of the varying-time signal itself by the dc blocker. However, this will increase the ternary filter order significantly and the advantage of simpler hardware would no longer be attainable. Consequently, we find it advantageous to

design the required ternary filter using three FIR filter design techniques to allow for performance comparison.

In all ternary filter design methods, we attempt to keep the filter order (and accordingly, the ternary taps) at a minimum. First, the well-known Remez Exchange technique has been utilized to generate a ternary filter of order 20. Then, the linear-phase FIR technique is adopted to get the benefit of a simpler hardware implementation due to symmetry/ anti-symmetry of the filter impulse response.

According to multi-rate processing theory, oversampling a signal compresses its spectrum. Hence, instead of directly designing a filter that satisfies the transition band specifications (i.e., f_{pass} and f_{stop}), an OSR -times-stretched specifications (i.e., $OSR * f_{\text{pass}}$ and $OSR * f_{\text{stop}}$) can be designed to meet these requirements. Thereafter, the filter order required to meet the new stretched band-edges will be remarkably lower than that designed to meet the original transition bands. Therefore, as our ternary- $\Sigma\Delta$ system is oversampled, an interpolated FIR (IFIR) approach is utilized to lower the required filter order that meet the target specifications. A comparison between these design techniques in terms of filter performance and hardware efficiency is then conducted in Section III.

B. The $\Sigma\Delta$ Modulator Stage

Spectral analysis of single-bit $\Sigma\Delta$ modulators with dc input has been addressed extensively in many works [9]-[11]. The results proved that when the input is steady, the white binary quantization noise assumption is not valid, and in fact it is highly colored, i.e., the noise has a discrete spectrum and it is not flat. By adopting the linear-model to represent the $\Sigma\Delta$ modulator, the power spectrum of its output with a dc input μ is given by [10]:

$$S_{yy}(f) = \frac{[2 \sin(\pi f)]^{2m}}{3} + \mu^2 \delta(f) \quad (3)$$

where f represents the normalized frequency and m is the order of the modulator. The second term of the righthand side of eq. (3) represents the input signal (dc in this case), whereas the first term represents the quantization noise introduced by the modulator. This means that the $\Sigma\Delta$ modulator transfers the original input dc value to its output and, in addition to that, presents a highly colored quantization noise. This is true as long as the input signal is within the modulator dynamic range (hence the system stability is maintained). This result will be utilized next.

C. Structure of the DC Blocker

Our objective is to design a structure to eliminate the dc content in a time-varying input signal. Fig.(3) depicts the proposed structure, firstly utilized in [12], to carry out this task. The structure consists of a ternary filter stage cascaded by IIR- $\Sigma\Delta$ modulator stage. The input to this structure, which is assumed a dc-biased sinusoidal signal, is assumed to be in single-bit format. The modulator stage encodes the multi-bit output of the ternary filter to single-bit format again. The ternary filter stage consists of $(M + 1) * OSR$ ternary taps.

Fig.(4) shows the linear model that represents the second-order $\Sigma\Delta$ modulator. The z-domain output transfer function of this model is given by:

$$Y(z) = G(z)z^{-1} + Q(z)(1 - z^{-1})^2 \quad (4)$$

where $G(z)$ and $Q(z)$ represent the signal and the quantization noise transfer functions, respectively. The noise shaping filter, $(1 - z^{-1})^2$, attenuates the quantization noise in the signal band and amplifies it outside the signal band. These high-frequency noise components can be eliminated by a subsequent digital decoding that also decimates the sample rate.

From 4, the frequency response is given by:

$$Y(e^{j\Omega}) = G(e^{j\Omega})e^{-j\Omega} + Q(e^{j\Omega})(1 - e^{-j\Omega})^2 \quad (5)$$

where $\Omega = 2\pi f/f_s$ is the normalized radian frequency. The output response of the overall system Y_{ov} will be the combination of the output frequency response of the ternary filter $Y_T(e^{j\Omega})$ and the frequency response of the IIR- $\Sigma\Delta$ modulator filter $H_{IIR}(e^{j\Omega})$ as follows:

$$Y_{ov}(e^{j\Omega}) = Y_T(e^{j\Omega}) \cdot H_{IIR}(e^{j\Omega}). \quad (6)$$

From (5) and (6) we get:

$$Y_{ov}(e^{j\Omega}) = Y_T(e^{j\Omega}) \cdot [H_{IIRS}(e^{j\Omega}) + H_{IIRN}(e^{j\Omega})] \quad (7)$$

where $H_{IIRS}(e^{j\Omega})$ and $H_{IIRN}(e^{j\Omega})$ are the signal and noise parts of $H_{IIR}(e^{j\Omega})$, respectively. Now, the overall output response, $Y_{ov}(e^{j\Omega})$, can be expressed as follows:

$$Y_{ov}(e^{j\Omega}) = \frac{G(e^{j\Omega}) K(e^{j\Omega})}{D(e^{j\Omega})} + \frac{Q(e^{j\Omega}) P(e^{j\Omega})}{D(e^{j\Omega})} \quad (8)$$

where

$$K(e^{j\Omega}) = e^{-j\Omega} + e^{-2j\Omega}(b - 2) + e^{-3j\Omega} \quad (9)$$

$$D(e^{j\Omega}) = 1 - ae^{-j\Omega} \quad (10)$$

$$P(e^{j\Omega}) = e^{-j\Omega}(b - 4) + e^{-2j\Omega}(6 - 2b) + e^{-3j\Omega}(b - 4) + e^{-4j\Omega}. \quad (11)$$

noting that a and b are the multiplication constants. The parameter a can be used to control the location of the overall function poles along the real z -axis and should be carefully set to insure correct operation and stability. The choice of a should ensure that the pole is located nearer to the origin than the zero. Also, the pole should not be faraway from the zero to ensure that no signal differentiation occurs, and a suitable gain is obtained.

The parameter b controls the amplitude of the input signal and can be adjusted to get maximum SNR. Fig.(5) depicts the theoretical frequency response of the signal-transfer function ($STF = K(e^{j\Omega})/D(e^{j\Omega})$) and the noise-transfer function ($NTF = P(e^{j\Omega})/D(e^{j\Omega})$) of the overall structure calculated from eq.(8).

III. SIMULATION AND DISCUSSION

MATLAB is utilized to simulate the proposed dc blocker. Fig.(6) shows the simulated frequency response of the ternary stage designed using Remez technique for the target response, in comparison with the calculated full-precision target response. There is an acceptable match between the two frequency response curves. It should be emphasized that the normalized frequency band of interest starts from about $\Omega=0.03\pi$ (for OSR = 32) and tends to the vicinity of 0 for higher OSR's. For a better presentation, the normalized radian frequency (Ω) axis is scaled from $\Omega=-0.1\pi$ to 0.1π .

As mentioned in Section-II, the ternary filter stage has been designed using three approaches. Figures (7), (8), and (9) show

Fig. 3. Structure of the proposed single-bit dc blocker.

Fig. 4. A block diagram of the linear model for a second-order $\Sigma\Delta$ modulator.

the simulated frequency response of the ternary stage using Remez, linear-phase (LP), and IFIR techniques, respectively.

Table-I compares the performance of these ternary filters in terms of signal and dc-content attenuation as well as hardware implementation efficiency. It is interesting to find out that the required transition band of the dc-blocker can be realized using only 70 ternary taps when IFIR design method is utilized. The price paid for this hardware simplicity is the increase in signal attenuation. It is worth noting that the zero-valued taps constitutes the majority of the total number of taps (64%-58%) in all cases.

Fig.(10) illustrates the phase response of the three ternary filters. As expected, the LP ternary filter possesses a linear phase response, a result which might be utilized for reducing the number of multipliers of the ternary filter. Fig.(11) shows the

Fig. 5. Frequency response of the theoretical STF (solid) and NTF (dotted) for $b=10$ and $a=0.001$.

TABLE I
A COMPARISON AMONG REMEZ, LINEAR-PHASE, AND IFIR TECHNIQUES.

Filtering Technique	Filter Order	Baseband Attenuation (dB)	DC Attenuation (dB)	No. of Ternary Taps	No. of Ternary Non-zero Taps	Percentage of zero Taps	Phase Response
Remez	21	2	35	672	282	58%	Linear
LP	19	2	28	640	232	64%	Linear
IFIR	7	5	35	193	70	64%	Piece-wise Linear

Fig. 6. Frequency response of the ternary filter stage (Remez) as compared to the target response (dashed line).

Fig. 7. Frequency response of the ternary filter stage using Remez technique, compared with the target response (dashed line).

Fig. 8. Frequency response of the ternary filter stage using linear-phase technique compared with the target response (dashed line).

Fig. 9. Frequency response of the ternary filter stage using IFIR technique.

Fig. 10. Phase response of the designed ternary filters: remez (solid), linear-phase (dashed), and IFIR (dotted).

impulse response curves of the linear-phase ternary filter and the full-precision target filter. It is obvious that the ternary filter has an anti-symmetric impulse response. This anti-symmetry can be utilized to halve the number of the coefficient multipliers [13]. Although ternary multipliers are simple in structure, it is still considered a remarkable reduction in hardware requirement in the case of linear-phase approach.

As was discussed before, when OSR increases, the signal spectrum approaches the frontier of the dc. In this case, the need for a larger order FIR filter becomes a vital demand. This can be deduced from Fig.(12), which shows the attenuation versus the OSR.

As discussed above [see eq.(3)], the $\Sigma\Delta$ modulator stage regulates the rate at which the output pulses occur attempting to keep the average output equal to the average input. Hence, it is anticipated that the $\Sigma\Delta$ modulator would preserve the dc content

Fig. 11. Impulse response of the linear-phase ternary filter stage and its full-precision counterpart.

Fig. 12. Signal attenuation in ternary filter stage against the OSR for $b = 1.6$ and $a = .01$. (*) Remez. (+) Linear-phase.

applied on its input as long as this dc is within its dynamic range. Fig.(13) shows the simulated overall filter frequency response as compared to the target response, using Remez ternary filter. It is clear that the proposed structure presents a good dc-blocking characteristics. Fig.(14) depicts the overall phase response along with that of the target phase response, where the overall phase response is deformed. This is expected due to the nonlinear behavior of the $\Sigma\Delta$ modulator stage. However, in the baseband, the phase response seems almost piecewise linear.

In Fig.(15), the input and the output spectra of the dc-blocker are shown. It is evident that the dc component in the input signal is removed completely. The input is taken as: $A_{dc} + A\sin(\omega_o t) + n(t)$, where $A_{dc} = 0.5$, $A = 0.5$, $\omega_o = 8192\pi$

Fig. 13. The overall frequency response of the ternary- $\Sigma\Delta$ M single-bit dc blocker.

Fig. 14. The overall phase response of the ternary- $\Sigma\Delta$ M single-bit dc blocker.

Fig. 15. Spectra of the single-bit input and the single-bit output of the proposed dc blocker. Above: input spectrum. Below: output spectrum.

rad/sec (chosen to be in the audio band), and $n(t)$ is an additive white Gaussian noise (AWGN). Hence, the input signal contains a dc power twice in magnitude as the sinusoidal power. To meet the minimum requirement for audio applications, the signal-to-noise ratio (SNR) is made 20 dB. Several different input types has also been used in testing the dc-blocker, such as sawtooth and FM. In all cases, the responses are comparable to those shown for the sinusoidal input.

The reconstructed dc-biased signals are shown in Fig.(16) and Fig.(17) for sinusoidal and sawtooth inputs, respectively. The reason behind utilizing the sawtooth input signal is to check for correctness of the system response by ensuring that differentiating to the input signal has not been taken place.

Fig. 16. Reconstructed sinusoidal dc-biased input signal from the single-bit dc blocker.

Fig. 17. Reconstructed sawtooth dc-biased input signal from the single-bit dc blocker.

IV. CONCLUSIONS

In this paper we proposed a dc-blocker in the single-bit domain. The dc-blocker consists of a ternary filtering stage and a sigma-delta modulator stage. Three design techniques were utilized to generate the ternary taps. For each technique, the associated ternary filter stage was assessed in terms of DC attenuation and hardware efficiency. The simulated system response has been studied through the application of various dc-biased, noisy signals. The dc content was removed completely from all kinds of input signals. The dc-blocker can be easily implemented with FPGA.

V. ACKNOWLEDGEMENT

This work is supported by the Australian Research Council under the ARC Discovery Grant DP0557429.

REFERENCES

- [1] F. Dachsel, and S. Quitzk, "Structure and information content in sequences from the single-loop sigma-delta modulator with dc input," *Proceedings of 2004 IEEE International Symposium on Circuits and Systems (ISCAS'04)*, pp. IV-685-688, May 2004.
- [2] S. Hein, "Tone suppression in general double-loop $\Sigma\Delta$ modulators using chaos," *IEEE International Symposium on Circuits and Systems (ISCAS)*, vol. 5, pp. 449-452, June 1994.
- [3] C. Dick, and F. Harris, "FPGA signal processing using sigma-delta modulation," *IEEE Signal Processing Magazine*, pp. 20-35, Jan. 2000.
- [4] A. C. Thompson, Z. M. Hussain, and P. O'Shea, "A Single-bit narrow-band Bandpass digital filter," *Australian Journal of Electrical and Electronics Engineering*, in press, 2005.
- [5] N. Benvenuto, L. E. Franks, and F. S. Hill, JR., "Realization of finite impulse response filters using coefficients +1, 0, -1," *IEEE Transactions on Communications*, vol. COM-33, no. 10, pp. 1117-1125, Oct. 1985.
- [6] B. R. Steele, *Efficient Signal Processing Through the Use of Sigma-Delta Modulation and Ternary Filters*, PhD dissertation, RMIT University, Melbourne, 2003.
- [7] A. C. Thompson, *Techniques in Single-Bit Digital Filtering*, PhD dissertation, RMIT University, Melbourne, 2004.
- [8] J. O. Smith III, *Introduction to digital filters with audio applications*, <http://ccrma.stanford.edu>, May 2004 draft.
- [9] J. C. Candy, and O. J. Benjamin, "The structure of quantization noise from sigma-delta modulation," *IEEE Transaction on Communications*, vol. COM-29, no. 9, pp. 1316-1323, Sept. 1981.
- [10] R. Gray, "Spectral analysis of quantization noise in a single-loop sigma-delta modulator with dc input," *IEEE Transaction on Communications*, vol. 37, no. 6, pp. 588-599, June 1989.
- [11] N. He, F. Kuhlmann, and A. Bunzo, "Double-loop sigma-delta modulation with dc input," *IEEE Transaction on Communications*, vol. 38, no. 4, pp. 487-495, April 1990.
- [12] A. C. Thompson, P. O'Shea, Z. M. Hussain, and B. R. Steele, "Efficient single-bit ternary digital filtering using sigma-delta modulator," *IEEE Signal Processing Letters*, vol. 11, no. 2, pp. 162-166, Feb. 2004.

[13] Z. M. Hussain, *Digital Signal Processing*, Lecture notes, RMIT University Press, 2004.