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Holland, A., Reeves, G., Matthews, G., & Leech, P. (2005). Finite element modeling of misalignment in interconnect vias. Proceedings of the 2004 Conference on Optoelectronic and Microelectronic Materials and Devices, 307–310. <https://doi.org/10.1109/COMMAD.2004.1577552>

Published Version: <https://doi.org/10.1109/COMMAD.2004.1577552>

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Finite Element Modeling of Misalignment in Interconnect Vias

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Abstract— Electrical resistance and hence heat generation in semiconductor chips are becoming more significant issues particularly as generations of silicon devices continue to have smaller features. The resistance of interconnect vias is a significant source of heat generation because of the increasing number of these on chips and increases in via resistance due to reduced size. Finite element modeling of voltage drops and current flow through interconnect vias gives information to aid in designing geometry and materials used in forming vias. It can also be used for modeling the thermal distribution in a via and hence the contribution by vias to heating a chip. In this paper we examine the effect of misalignment of the via between the two metal layers M1 and M2 with regard to the interconnect via resistance. The effect of the interface specific contact resistance is examined in particular. Significant misalignment can be tolerated without increasing the via resistance. The heat generation due to electrical current flow in the via materials and interfaces is modelled using the same finite element mesh and software. The output of the electrical analysis is used as the heat generation input for the thermal analysis.

Keywords: *Interconnect, via, contact resistance, Finite Element, NASTRAN*

I. INTRODUCTION

Reduction in interconnect via resistance is desirable to minimise the heat that such structures generate in semiconductor chips. As shown in Figure 1 there are several materials in an via structure and considering the material properties (particularly electrical conductivity and thermal conductivity) and the geometry there are many combinations for determining via resistance. An interconnect via (like an ohmic contacts) should allow the supply of appropriate electrical current for fundamental operations of a semiconductor chip without affecting the electrical characteristics of the circuit [1]. However, via dimensions are reducing with every successive generation of silicon semiconductor technology. By using Finite element analysis we can optimise the use of material and geometries of interconnect to minimise via resistance. The electrical equation used to describe d.c. electrical conduction (equation 1) is analogous to that for thermal conduction. the equation (equation 2)

$$J = \sigma dV/dn \quad (1)$$

where

J = electrical current density

V = voltage

n = spatial coordinate in the direction of current flow

σ = material electrical conductivity

$$H = k dT/dn \quad (2)$$

where

H = heat flux

T = temperature

n = spatial coordinate in the direction of current flow

k = material thermal conductivity

Equations 1 and 2 have the same form and therefore can be solved using the same finite element program.

II. DEVICE STRUCTURE

Figure 1 shows a three dimensional finite element mesh used for modelling an interconnect via. Figure 2 shows a close-up view of the bottom section of the model. NASTRAN is a finite element program developed by NASA for heat transfer analysis (and mechanical structural analysis). Nathan et al. [2] reported on the use of this program for electrical analysis based on the analogy indicated by equations 1 and 2. In this paper we report on the use of NASTRAN for modelling electrical interconnect vias in silicon devices and examine the effect of via misalignment on the resistance of the via. The electrical current density in any material is a source of heat generation. Using NASTRAN for solving heat transfer and with the electrical current density heat generation as an input we can model heat transfer in the via and temperature distribution due to electrical current flow. Each interface in the via i.e. the interface between M1 and the liner and between M2 and the liner has its own value of specific contact resistance ρ_c ($\Omega \cdot \text{cm}^2$)

Figure 1. Cross-section of finite element mesh used for modelling electrical current flow from Metal layer M1 to M2 in a semiconductor interconnect via.

Figure 2. Close-up view of bottom section of finite element mesh via. Five materials are shown including the two interfaces which are modelled as being 20 Angstroms thick.

as for any two layer ohmic contact. Berger [3] suggested that such an interface has a thickness of 10nm. This is rather large considering the dimensions of liners used in vias. We have modelled the interface as having a thickness of 2nm. By giving the 2nm thick interface material an effective electrical resistivity ($\Omega\cdot\text{cm}$, $1/\sigma$) value we can model for the correct specific contact resistance value for any interface. By changing the resistivity of this interface we can model for the effect of varying values of ρ_c . This material property of any ohmic contact interface can vary by orders of magnitude and despite it consisting of only a small percentage of the via volume it can have a significant effect on overall via resistance. It can influence the current distribution in M1, the liner and M2. In particular for the electrical current distribution in M1 the value of the specific contact resistance for the M1/liner interface (ρ_{c1}) can influence the effect of misalignment on the via resistance. Figure 2 shows a close-up view of the bottom of the via model and in this region the three materials are in close proximity to each other.

Sabelka and Selberherr [4] modelled the via resistance of a copper via and found the measured experimental value to be 30% larger than that determined by their finite element model. They attributed this difference to the fact that they did not account for the ohmic contact interfaces in their via model. Until the values of specific contact resistance of each two layer ohmic interface is determined experimentally we cannot accurately model interconnect via structures. However reasonable estimates can be made based on via resistances measured. For example if the via structure shown in Figure 1 gives an experimentally determined via resistance R_v of 5Ω then we know that $\rho_{c1} < 1 \times 10^{-8} \Omega\cdot\text{cm}^2$. This can be determined by running finite element analysis knowing all other parameters i.e. device geometry, resistivities and R_v .

III. SIMULATION RESULTS

The liner thickness is 50nm. A circularly shaped via is modelled. The bottom of the via plug has an inner diameter of 200nm. Typical cross-sections of interconnect vias would show a cross-section that had rounded corners even if the nominal geometry was for a square cross-section. The via aspect ratio is approximately 6 and the thickness of M1 and M2 are 0.2 and 0.3 μm respectively. The resistivity of thin films are typically higher than the pure material resistivity. Values of 4 and 3 $\mu\Omega\cdot\text{cm}$ were chosen for M1 and M2 respectively. The liner resistivity was chosen to represent a typical TiN value. This was 100 $\mu\Omega\cdot\text{cm}$. For initial modelling of via resistance for misalignment estimates for ρ_{c1} and ρ_{c2} were used. These were both chosen to be $1 \times 10^{-9} \Omega\cdot\text{cm}^2$. As far as the authors are aware there are no experimental values reported for the specific contact resistance for these interfaces. The input current is 1mA.

A. VARIATION IN VIA RESISTANCE

Using the model described above the via was misaligned to various degrees with the metal layer M1. This was normalised to the diameter d of the M1/liner interface i.e. misalignment

varied from 0 to d . The diameter d in Figure 3 is $0.3\mu\text{m}$. Table 1 shows values of via resistance R_v for different amounts of misalignment for the via parameters given in Section II. The effect of ρ_{c1} is significant in determining R_v . The values used are close to the actual values which are unknown but can be estimated from known values of R_v as described above. Further experimental work is required to determine the specific contact resistance of each interface encountered in semiconductor vias in order to undertake more accurate modelling. Experimental test structures such as described in [6] are suitable for measuring low values of ρ_c .

Figure 3. Schematic showing how the misalignment of the interconnect was modelled. The circle with the solid line indicates perfect alignment.

TABLE I. VIA RESISTANCE R_v FOR VARYING MISALIGNMENT

Misalignment (units of diameter d)	$R_v (\Omega)$ $\rho_{c1} = 1 \times 10^{-9} \Omega \cdot \text{cm}^2$	$R_v (\Omega)$ $\rho_{c1} = 1 \times 10^{-9} \Omega \cdot \text{cm}^2$
0	18.3	3.9
0.25d	18.3	3.9
0.50d	18.3	3.9
0.75d	18.8	4.4
1.00d	21.2	6.8

As shown in Table 1 the effect of misalignment on via resistance is negligible if all of the liner bottom area is in contact with M1. The via resistance only increases when the contact area reduces because of significant misalignment. This is because the resistance due to the interface is relatively large compared with the M1 layer and this determines the current distribution under the via. The liner can also influence this. The current distributes uniformly below the M1/liner interface to minimise resistance. This can be clearly seen in Figure 4 where at the bottom of the via the equipotentials are seen to be all parallel with the M1/liner interface. This indicates that the current through this interface has distributed uniformly to minimise the resistance. This was for $\rho_{c1} = 1 \times 10^{-9} \Omega \cdot \text{cm}^2$ and for any larger values the distribution will be similar. Even if the value of ρ_{c1} was lower the distribution will be similar because of the effect of the relatively resistive liner. From Table 1 and

Figure 4 we can assume that the current through ρ_{c1} is uniform and therefore the resistance contributed is approximately 1.4Ω for the case where $\rho_{c1} = 1 \times 10^{-9} \Omega \cdot \text{cm}^2$ and this is a significant percentage of the via resistance. This would account for some of the error observed ref. [4] where such interfaces were not modelled. Further resistance will be due to the presence of the interface ρ_{c2} .

Figure 4. Equipotential distribution in the interconnect via model described in section III.

B. HEAT GENERATION IN VIA

The same model used to determine the equipotential and electrical current distribution can be used to determine the temperature and heat flow distribution in the via. The input for this is the heat generated in each element of the finite element via model due to Joule heating. When an electrical current flows through a semiconductor bulk material, it generates Joule heat power of density

$$G = j^2 \times \rho_b \quad (3)$$

Where j is current density (Amp/cm^2), ρ_b is the bulk electrical resistivity ($\Omega \cdot \text{cm}$) and the units of G is W/cm^3 . j is an output of the electrical analysis for each element of the model. By modifying this output using equation 3 then the heat generation in the via can be defined. By defining the conductivity of the materials in the via structure to now be the thermal conductivity then equation 2 can be solved to obtain the temperature and heat flow distribution. The thermal conductivities were as follows

Al: 2.37 W/cm/K
 TiN: 0.28 W/cm/K
 Cu: 4.00 W/cm/K

Running this analysis using NASTRAN shows that for a current of 1mA the temperature difference across the via structure is up to 35 K. In order to minimise this, lower electrical resistive materials are required especially for the liner and the values of the specific contact resistance will also have to be minimised. Heat sinking dielectric materials will also reduce this heating.

IV. CONCLUSIONS AND FUTURE WORK

The finite element program NASTRAN was developed to model structural and heat flow analysis. Here we have used it to analyse the heat flow in a semiconductor interconnect via structure due to electrical current flow through the different materials of the via. By including the interfaces in the model it is shown that these can significantly influence the via resistance. By analogy we used the program to model

electrical current flow and then used this as the source of heat generation for input into the heat flow analysis.

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